CLAIM AMENDMENTS

Claims 1-26 are pending and under consideration. Please amend claims 1, 2, 3, 10, 17 and 26. Please add new claim 27. No new matter is introduced. The claim listing below will replace all prior versions of claims in the application.

1. (Currently Amended) A method for performing time slot switching of synchronous data across an asynchronous packet switch comprising:

(a) converting time-sensitive synchronous serial data related to a plurality of source time slots in a time-division multiplexing frame into synchronous parallel data units in accordance with a synchronous clock signal;

(b) formatting the synchronous parallel data units into at least a first subpacket and a second subpacket in accordance with the synchronous clock signal, the first subpacket and the second subpacket being generated during a first synchronization interval of the synchronous clock signal, the first subpacket being associated with a first source time slot in the time-division multiplexing frame and comprising ~~an ingress queue identifier and~~ data corresponding to a first destination time slot identifier and the second subpacket being associated with a second source time slot in the time-division multiplexing frame and comprising ~~the same ingress queue identifier and~~ data corresponding to a second destination time slot identifier;

(c) generating a packet from a plurality of subpackets ~~sharing the same ingress queue identifier,~~ including the first subpacket and the second subpacket, the packet comprising data corresponding to a synchronization tag identifying the synchronization interval in which the first subpacket and the second subpacket were formatted;

(d) asynchronously transmitting the packet across the asynchronous packet switch; and

(e) extracting the subpackets from the packet and storing the subpackets in a first buffer and a second buffer based on the data corresponding to the first destination time slot identifier and data corresponding to the second destination time slot identifier stored within the respective subpackets, the first buffer being associated with the first destination time slot and the second buffer being associated with the second destination time slot, the arrangement of subpackets within the first buffer and the second buffer being determined by data corresponding to a

synchronization tag identifying the ~~first~~ synchronization interval during which the subpacket was generated plus a known fixed delay offset.

2. (Currently Amended) An apparatus for performing time slot switching of synchronous data across an asynchronous packet switch comprising:

(a) serial to parallel interface for converting time-sensitive synchronous serial data related to a plurality of source time slots in a time-division multiplexing frame into synchronous parallel data units in accordance with a synchronous clock signal;

(b) a logic circuit for formatting the synchronous parallel data units into at least a first subpacket and a second subpacket in accordance with the synchronous clock signal, the first subpacket and second subpacket being generated during a first synchronization interval of the synchronous clock signal, the first subpacket being associated with a first source time slot in the time-division multiplexing frame and comprising ~~an ingress queue identifier and~~ data corresponding to a first destination time slot identifier and the second subpacket being associated a second source time slot in the time-division multiplexing frame and comprising ~~the same ingress queue identifier and~~ data corresponding to a second destination time slot identifier;

(c) a logic circuit for generating a packet from a plurality of subpackets ~~sharing the same ingress queue identifier,~~ including the first subpacket and second subpacket, in an ingress queue coupled to the asynchronous packet switch, the packet comprising data corresponding to a synchronization tag identifying the synchronization interval in which the first subpacket and the second subpacket were formatted;

(d) a logic circuit for asynchronously transmitting the packet across the asynchronous packet switch, to a packet switch output port in communication with a plurality of destination time slots corresponding to at least the first time slot and the second source time slot;

(e) a logic circuit for extracting the subpackets from the packet and for storing the subpackets into a first buffer and a second buffer based on the data corresponding to the first destination time slot identifier and data corresponding to the second destination time slot identifier stored within the respective subpackets, the first buffer being associated with the first destination time slot and the second buffer being associated with the second destination time slot,

the arrangement of subpackets within each of the first and second buffer being determined by a value representing the first synchronization interval plus a known fixed delay offset.

3. (Currently Amended) A method for transferring data comprising:

(a) packetizing a plurality of time-sensitive synchronous serial data streams relating to a plurality of source time slots in a time-division multiplexing frame into a respective first subpacket and second subpacket during a first synchronization interval, the first subpacket being associated with a first source time slot in the time-division multiplexing frame and comprising ~~an ingress queue identifier and~~ data corresponding to a first destination time slot identifier and the second subpacket being associated with a second source time slot in the time-division multiplexing frame and comprising ~~the same ingress queue identifier and~~ data corresponding to a second destination time slot identifier;

(b) asynchronously transmitting at least the first subpacket and second subpacket through an asynchronous packet switch; and

(c) reconverting the first subpacket and second subpacket, based on the data corresponding to the first destination time slot identifier and data corresponding to the second destination time slot identifier stored within the respective first subpacket and second subpacket, into synchronous data streams comprising a first data stream associated with a first destination time slot and a second data stream associated with a second destination time slot, the first subpacket and the second subpacket reconverted during a second synchronization interval having a known fixed delay offset relation to the first synchronization interval.

4. (Original) The method of claim 3 wherein (a) comprises:

(a1) converting the synchronous serial data streams into synchronous parallel data units.

5. (Previously Presented) The method of claim 4 wherein (a) comprises:

(a2) formatting the synchronous parallel data units into respective subpackets during a first synchronization interval.

6. (Original) The method of claim 5 wherein (b) comprises:

(b1) generating a packet from a plurality of subpackets, the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data units, and a destination time slot identifier associated with each subpacket.

7. (Previously Amended) The method of claim 6 wherein (b) comprises:

(b2) asynchronously transmitting the subpackets through an asynchronous packet switch as part of the packet.

8. (Original) The method of claim 3 wherein (c) comprises:

(c1) extracting the subpackets from the packet, and

(c2) storing the subpackets into a plurality of buffers, each of the buffers associated with a destination time slot, the arrangement of subpackets within the buffers being determined by a value representing the first synchronization interval plus a fixed delay offset.

9. (Original) The method of claim 8 wherein (c) comprises:

(c3) reading the subpackets from the buffers as a plurality of parallel data units; and

(c4) converting the parallel data units into synchronous serial data streams.

10. (Currently Amended) An apparatus for transferring data comprising:

(a) a source of synchronization signals defining a plurality synchronization intervals;

(b) an interface for packetizing a plurality of synchronous data streams relating to source time slots in a time-division multiplexing frame into respective first subpacket and second subpacket during a first synchronization interval, the first subpacket associated with a first source time slot in a time-division multiplexing frame and comprising ~~an ingress queue identifier and~~ data corresponding to a first destination time slot identifier and the second subpacket associated with a second source time slot in a time-division multiplexing frame and comprising ~~the same ingress queue identifier and~~ data corresponding to a second destination time slot identifier;

(c) a mechanism for asynchronously transmitting the first subpacket and second subpacket through an asynchronous packet switch; and

(d) an interface for reformatting the first subpacket and second subpacket, based on the data corresponding to the first destination time slot identifier and data corresponding to the second destination time slot identifier stored within the respective subpackets, into synchronous data streams comprising a first data stream being associated with a first destination time slot and a second data stream being associated with a second destination time slot, the first subpacket and the second subpacket reformatted during a second synchronization interval having a known and fixed delay offset relation to the first synchronization interval.

11. (Original) The apparatus of claim 10 wherein (b) comprises:

(b1) logic for converting the synchronous serial data streams into synchronous parallel data units.

12. (Original) The apparatus claim 11 wherein (b) comprises:

(b2) logic for formatting the synchronous parallel data units into a subpackets during a first synchronization interval.

13. (Original) The apparatus of claim 12 wherein (b) comprises:

(b3) logic for generating a packet from a plurality of subpackets, the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data units, and a destination time slot identifier associated with each subpacket.

14. (Previously Cancelled)

15. (Original) The apparatus of claim 10 wherein (d) comprises:

(d1) logic for extracting the subpackets from the packet, and

(d2) logic for storing the subpackets into a plurality of buffers, each of the buffers associated with a destination time slot, the arrangement of subpackets within the buffers being determined by a value representing the first synchronization interval plus a fixed delay offset.

16. (Original) The apparatus of claim 15 wherein (d) comprises:

(d3) logic for reading the subpackets from the buffers as a plurality of parallel data units; and

(d4) logic for converting the parallel data units into synchronous serial data streams.

17. (Currently Amended) An apparatus comprising:

(a) an asynchronous packet switch;

(b) a plurality of circuit server modules coupled to the asynchronous packet switch, the server modules comprising: (i) a time division multiplex interface; and (ii) data adaptation logic; and

(c) a source of synchronous clock signals coupled to each of the circuit server modules, the synchronous clock signals defining a plurality of synchronization intervals;

the circuit server modules configured to perform synchronous time slot switching of synchronous data in a time-division multiplexing frame across the asynchronous packet switch by asynchronously transmitting packets of the synchronous data across the asynchronous packet switch, the packets comprising at least a first subpacket being associated with a first source time slot in a time-division multiplexing frame and comprising ~~an ingress queue identifier and~~ data corresponding to a first destination time slot identifier and a second subpacket being associated with a second source time slot in a time-division multiplexing frame and comprising ~~the same ingress queue identifier and~~ data corresponding to a second destination time slot identifier.

18. (Original) The apparatus of claim 17 wherein the time division multiplex interface comprises: serial to parallel conversion logic for converting synchronous serial data streams into parallel data units.

19. (Original) The apparatus of claim 17 further comprising: parallel-to-serial conversion logic for converting a plurality of parallel data units into synchronous serial data streams.

20. (Original) The apparatus of claim 18 wherein the data adaptation layer comprises:
an ingress data memory coupled to the time division multiplexed interface;
an ingress context memory; and

subpacket construction logic for constructing in the ingress data memory a plurality of subpackets during one of the synchronization intervals, each subpacket associated with a source time slot and containing parallel data derived from a synchronous serial data stream received through the time division multiplexed interface subpacket.

21. (Original) The apparatus of claim 20 wherein the ingress context memory stores context data associated with a subpacket, the context data comprising a destination time slot identifier and a queue identifier associated with a subpacket.

22. (Previously Amended) The apparatus of claim 21 wherein the data adaptation layer comprises:

an ingress queue coupled to the asynchronous packet switch; and

packet construction logic for constructing in the ingress queue a packet including a plurality of subpackets and the respective context data associated with each subpacket.

23. (Original) The apparatus of claim 22 wherein the packet further comprises data identifying the synchronization interval during which the subpackets contained therein were constructed.

24. (Previously Amended) The apparatus of claim 17 wherein the data adaptation layer further comprises:

an egress data memory having a plurality of playout buffers associated with a plurality of destination time slots; and

depacketizing logic for receiving a packet from the asynchronous packet switch and for storing subpackets contained therein into the plurality of playout buffers in the egress data memory.

25. (Original) The apparatus of claim 24 wherein the data adaptation layer further comprises:

playout logic for synchronously supplying parallel data from the playout buffers to the time division multiplexed interface.

26. (Currently Amended) A memory for storing data to be processed by a data processing system including an asynchronous packet switch, the memory comprising:

a data structure stored in the memory and usable to perform time slot switching of data, the data structure comprising:

a packet comprising ~~a plurality of subpackets~~ comprising at least a first subpacket associated with a first source time slot in a time-division multiplexing frame and comprising ~~an ingress queue identifier and~~ data corresponding to a first destination time slot identifier associated with a first buffer; and a second subpacket associated with a second source time slot in a time-division multiplexing frame and comprising ~~the same ingress queue identifier and~~ data corresponding to a second destination time slot identifier associated with a second buffer, the plurality of subpackets containing parallel data derived from a synchronous serial data stream, each subpacket constructed during a common synchronization interval;

data corresponding to a synchronization tag in the packet identifying the common synchronization interval during which the plurality of subpackets were constructed and determining the arrangement of the plurality of subpackets within the first buffer and the second buffer; and

data in the packet identifying the number of subpackets contained within the data structure,~~; and~~

~~context data associated with each one of the plurality of subpackets, the context data including the first destination time slot identifier corresponding to the first source time slot in a time-division multiplexing frame associated with the first subpacket and a second destination time slot identifier corresponding to the second source time slot in the time division multiplexing frame associated with the second subpacket.~~

27. (New) A computer program product, tangibly embodied in a computer-readable storage device, the computer program product including instructions being operable to cause a computing device to:

convert time-sensitive synchronous serial data related to a plurality of source time slots in a time-division multiplexing frame into synchronous parallel data units in accordance with a synchronous clock signal;

format the synchronous parallel data units into at least a first subpacket and a second subpacket in accordance with the synchronous clock signal, the first subpacket and the second subpacket being generated during a first synchronization interval of the synchronous clock signal, the first subpacket being associated with a first source time slot in the time-division multiplexing frame and comprising data corresponding to a first destination time slot identifier and the second subpacket being associated with a second source time slot in the time-division multiplexing frame and comprising data corresponding to a second destination time slot identifier;

generate a packet from a plurality of subpackets including the first subpacket and the second subpacket, the packet comprising data corresponding to a synchronization tag identifying the synchronization interval in which the first subpacket and the second subpacket were formatted;

asynchronously transmit the packet across the asynchronous packet switch; and

extract the subpackets from the packet and storing the subpackets in a first buffer and a second buffer based on the data corresponding to the first destination time slot identifier and data corresponding to the second destination time slot identifier stored within the respective subpackets, the first buffer being associated with the first destination time slot and the second buffer being associated with the second destination time slot, the arrangement of subpackets within the first buffer and the second buffer being determined by data corresponding to a synchronization tag identifying the synchronization interval during which the subpacket was generated plus a known fixed delay offset.